Remarks/Arguments

Reconsideration of this application is requested.

Claim Status

Claims 1-17 are pending in this application and remain pending after this amendment. Claims 1, 2, 9, 10 and 12-15 are amended.

Allowable Subject Matter

The indication of allowable subject matter in claim 5 is noted and appreciated.

Claim Objections

Claims 10-17 are objected to. The Action asserts that claims 10 and 12-15 seem to be independent claims depending from other independent claims. In response, claims 10 and 12-15 are rewritten in independent form. Applicant submits that the objection to claims 10-17 should be withdrawn.

Claim Rejections – 35 USC 102

Claims 1-4 and 6-17 are rejected under 35 USC 102(e) as anticipated by U.S. patent 6,438,035 to Yamamoto et al. As claim 1 includes multiple limitations that are not shown or suggested by Yamamoto, applicant respectfully traverses these rejections.

The Action asserts that reference memory cell RMC 2 of Yamamoto (Fig. 1) meets the requirements of claim 1 of a second memory cell adjacent to a first memory cell and written after the first memory cell. Applicant respectfully disagrees.

First, Yamamoto discloses a memory cell array 1 constructed of a plurality of memory cells MC00 through MC12. As is evident in Yamamoto's Fig. 1, RMC 2 (which the Action asserts as corresponding to the claimed second memory cell) is not part of array 1. It is separate and remote from array 1. Claim 1, conversely, requires that the memory cells (first and second) be arranged in and selected from the memory cell array. Since Yamamoto's second memory cell (RMC 2) is not formed in a memory cell array, Yamamoto cannot anticipate claim 1.

Second, Yamamoto's asserted second memory cell RMC 2 is not formed *adjacent to the first memory cell* as is required by claim 1. RMC 2 is connected to a precharge circuit 3 and a reference cell sense amplifier section 5 through a reference bit line RBL, while normal (first) memory cells MC00...MC12 are connected to normal bit lines BL0, BL1 and BL2, which are connected to a precharge circuit 7, sense amplifier section 8 and Y decoder 10. Since Yamamoto does not disclose a second memory cell adjacent to a first memory cell, Yamamoto cannot anticipate claim 1.

Finally, RMC 2 is clearly not written after a first memory cell, as is required by claim 1. As stated at Yamamoto, column 8, lines 35-40:

> The reference cell 2 for the read operation has its threshold voltage set to a threshold voltage Vref at the middle of a threshold voltage of the state 1 and a threshold voltage of the state 0. This setting is achieved by *preliminarily* alternately executing write operation with write pulses and verify operation in a reference cell 2.

Clearly, RMC 2 is not written after a first memory cell. Yamamoto cannot anticipate claim 1 for this reason as well.

Conclusion

This application is now believed to be in form for allowance. The examiner is invited to telephone the undersigned to resolve any issues that remain after entry of this amendment. Any fees due in connection with this response, including fees for extra claims, may be charged to our Deposit Account No. 50-1314.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

Date: October 27, 2004

By:_____

Troy M. Schmelzer
Registration No. 36,667
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701